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1 A compiler-directed cache coherence scheme with improved intertask locality

Choi, L.; Pen-Chung Yew;

Supercomputing '94. Proceedings , 14-18 Nov 1994

Page(s): 773 -782

[\[Abstract\]](#) [\[PDF Full-Text \(748 KB\)\]](#) **IEEE CNF**

2 A timestamp-based selective invalidation scheme for multiprocessor cache coherence

Xin Yuan; Melhem, R.; Gupta, R.;

Parallel Processing, 1996., Proceedings of the 1996 International Conference on , Volume: 3 , 12-16 Aug 1996

Page(s): 114 -121 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(792 KB\)\]](#) **IEEE CNF**

3 Design and analysis of a scalable cache coherence scheme based on clocks and timestamps

Min, S.L.; Baer, J.-L.;

Parallel and Distributed Systems, IEEE Transactions on , Volume: 3 Issue: 1 , Jan 1992

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[\[Abstract\]](#) [\[PDF Full-Text \(1560 KB\)\]](#) **IEEE JNL**

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L2: Entry 7 of 7

File: USPT

Jul 9, 1996

DOCUMENT-IDENTIFIER: US 5535366 A

TITLE: Method of and circuit arrangement for freeing communications resources,
particularly for use by a switching elementCurrent US Original Classification (1):711/159Current US Cross Reference Classification (1):711/151Current US Cross Reference Classification (2):711/158Current US Cross Reference Classification (3):711/160Other Reference Publication (5):S-L Min et al; "A Timestamp-based Cache Coherence Scheme" Proc. 1989 Intern'l Conf.
on Parallel Process'g; vol. 1, pp. I23-I32; 8 Aug. '89.

<u>L25</u>	l4 and (((dasd or disk or (storage adj2 device)) with cach\$3) with (map\$1 or mapping))	48	<u>L25</u>
<u>L24</u>	l4 and (((dasd or disk or (storage adj2 device)) with cach\$3) same (map\$1 or mapping))	82	<u>L24</u>
<u>L23</u>	l18 and (database or data-base or (data adj2 base))	0	<u>L23</u>
<u>L22</u>	L20 and (time or time-stamp\$3 or timestamp\$3 or (time adj2 stamp\$3))	1	<u>L22</u>
<u>L21</u>	L20 and (time or time-stamp\$3 or timestamp\$3)	1	<u>L21</u>
<u>L20</u>	5418921.pn.	1	<u>L20</u>
<u>L19</u>	L18 and database	0	<u>L19</u>
<u>L18</u>	4603380.pn.	1	<u>L18</u>
<u>L17</u>	L16 and l15	1	<u>L17</u>
<u>L16</u>	L13 and (map\$1 or mapping)	2	<u>L16</u>
<u>L15</u>	L13 and (lru or (least adj2 recently adj2 used))	3	<u>L15</u>
<u>L14</u>	L13 and (timestamp\$3 or time-stamp\$3 or (time adj2 stamp\$3))	0	<u>L14</u>
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<u>L11</u>	((711/113)!.CCLS.)	541	<u>L11</u>
<u>L10</u>	L9 and database	0	<u>L10</u>
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<u>L8</u>	L4 and (((dasd) with cach\$3) same (time-stamp\$3 or (time adj2 stamp\$3)))	2	<u>L8</u>
<u>L7</u>	L4 and (((dasd) with cach\$3) with tim\$3)	34	<u>L7</u>
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<u>L1</u>	((711/167)!.CCLS.)	724	<u>L1</u>

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Term:

117 and ((request\$3) adj2 (queue\$3 or buffer\$3))

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side by side

Hit Count Set Name

result set

DB=USPT; PLUR=YES; OP=OR

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<u>L18</u>	L15 and ((queue\$3 or buffer\$3) same (lock\$3 with (concurrent\$2 or simultaneous\$2)))	1	<u>L18</u>
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<u>L16</u>	L15 and ((concurrent\$2 or simultaneous\$2) same ((request\$3) adj2 (queue\$3 or buffer\$3)))	17	<u>L16</u>
<u>L15</u>	((711/144 711/145)!.CCLS.)	690	<u>L15</u>
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<u>L13</u>	((711/168)!.CCLS.) and ((concurrent\$2 or simultaneous\$2) same ((request\$3) adj2 (queue\$3 or buffer\$3)))	11	<u>L13</u>
<u>L12</u>	((711/168)!.CCLS.) and ((concurrent\$2 or simultaneous\$2) same ((request\$3) adj2 (queue\$3 or buffer\$3)))	11	<u>L12</u>
<u>L11</u>	((711/168)!.CCLS.) and ((request\$3) adj2 (queue\$3 or buffer\$3))	44	<u>L11</u>
<u>L10</u>	L7 and ((request\$3) adj2 (queue\$3 or buffer\$3))	73	<u>L10</u>
<u>L9</u>	L7 and ((access\$3 or request\$3) adj2 (queue\$3 or buffer\$3))	96	<u>L9</u>
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<u>L6</u>	L5 and ((request\$3 or access\$3) adj2 (queue or buffer\$3))	0	<u>L6</u>
<u>L5</u>	5806085.pn. or 6449695.pn. or 6532521.pn. or 6532490.pn.	4	<u>L5</u>
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<u>L3</u>	L2 and ((data or datum or line or entry) with (expir\$5 or timeout or time-out or timing-out))	114	<u>L3</u>
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